PATENT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

APPLICANTS:	Cook et al.	DKT NO:	YOR9-2000-0402US1 (8728-497)
SERIAL NO.:	09/836,375	ART UNIT:	2115
FILED:	17 April 2001	EXAMINER:	Suryawanshi, Suresh.

ON: LATCH STRUCTURE FOR INTERLOCKED PIPELINED CMOS (IPCMOS) CIRCUITS

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RULE 132 DECARATION

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence (and any document referred to as being attached or enclosed) is being deposited with the United States Postal Service as first class mail, postage paid in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313 on the date indicated below:

Date: June 30, 2004 By: [signature]

Peter W. Cook and Stanley E. Schuster declare as follows:

1. We are the inventors of the above-referenced application, and we have reviewed the Office Action dated 02 April 2004, and the reference cited as prior art, "Asynchronous Interlocked Pipelined CMOS Circuits Operating at 3.3-4.5GHz" appearing in *ISSCC 2000/Session 17/Logic and Systems/ Paper WA 17.3*, presented on February, 2000, and authored by Stanley Schuster, William Reohr, Peter Cook, David Heidel, Michael Immediato, Keith Jenkins (hereinafter the "Article").

2. The Article was published at the 2000 IEEE International Solid-State Circuits Conference. We are two of the six authors of the Article. The other four authors of the Article (William Reohr, David Heidel, Michael Immediato, Keith Jenkins) were working under our direction and supervision constructing and testing the subject matter described in the article. Any knowledge they had of the subject matter described in the article was derived from us.

We HEREBY DECLARE that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 U.S. Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Peter W. Cook

Peter W. Cook

Date: 6/29/04

Stanley E. Schuster

Stanley E. Schuster

Date: 6/29/04